WHAT IS CLAIMED IS:

1. A bus manager comprising:

at least one bus;

a plurality of bus masters connected to said bus;

first storage means for storing conditions for starting and conditions for ending granting of bus use privilege to each of said plurality of bus masters; and

bus arbitration means for granting said plurality of bus masters the bus use privilege or depriving said plurality of bus masters of the bus use privilege in accordance with the conditions if there are bus use requests from said plurality of bus masters.

2. The bus manager according to claim 1, further comprising second storage means for storing an order of said plurality of bus masters, wherein said bus arbitration means grants bus use privilege to a bus master which satisfies the order and the starting conditions and deprives a bus master which satisfies the ending conditions of the bus use privilege.

3. The bus manager according to claim 1, further comprising mode setting means capable of setting a priority sequential mode and a complete sequential mode, wherein:

in the priority sequential mode, said bus arbitration means grants a bus master, whose conditions for starting and conditions for ending granting of bus use privilege have been stored in said first storage means, the bus use privilege at a priority higher than that other bus masters; and

in the complete sequential mode, said bus arbitration means refrains from granting bus use privilege to a bus master whose conditions for starting and conditions for ending granting of bus use privilege have not been stored in said first storage means.

4. A bus manager comprising:

at least four buses;

bus masters connected to said buses; and

changeover means for changing over a connection among said buses in conformity with bus requests from bus masters connected to respective ones of said buses.

5. The bus manager according to claim 4, wherein a memory is connected to one of said at least four buses, and at least one bus master is connected to each of the other buses.

6. The bus manager according to claim 5, wherein said other buses include a bus connected to a memory, a bus connected to a processor, and at least two buses connected to an input/output device, and said changeover means performs arbitration between a connection request from the bus connected to the memory and connection requests from the buses connected to the input/output device.

7. The bus manager according to claim 6, wherein said changeover means connects, in parallel, a pair consisting of the bus connected to said memory and one of the buses connected to said input/output device and a pair consisting of the bus connected to said processor and the other of the

buses connected to said input/output device.

8. The bus manager according to claim 6, wherein said changeover means performs arbitration between a connection request, from said processor, for connection to a memory or input/output, and a connection request, from each input/output bus, for connection to the memory.

9. The bus manager according to claim 4, further comprising a controller for controlling an image input/output device which inputs and outputs image data, said controller being connected to two buses connected to said input/output device.

10. A bus manager comprising:

at least two buses each having a bus master;

a memory accessed via said buses;

arbitration means connected to respective ones of said buses for arbitrating bus requests from the bus masters of the corresponding buses and granting bus use privilege to any of the bus masters; and

bus synchronizing means operable, in a case where a plurality of bus masters that have been granted bus use privilege with respect to the respective buses write data to the same destination, for so notifying the arbitration means so that the arbitration means will stop the granting of the bus use privilege to the bus masters with the exception of a bus master that issued a bus request first.

11. The bus manager according to claim 10, wherein said bus synchronizing means stores a time at which a bus request has

been issued by each of said plurality of bus masters, compares addresses specified together with the bus requests from each of the bus masters, compares the stored times if the addresses match and halts the bus masters with the exception of a bus master that issued a bus request at the earliest time.

12. A bus manager comprising:

at least two buses each having bus arbitration means;

bus masters connected to said buses; and

decision means for judging status of each of said buses and information relating to bus requests issued by said bus masters, and deciding which of said buses should be used.

13. The bus manager according to claim 12, wherein the information relating to bus requests includes degree of priority of the bus request, transfer destination of data and transfer size, the status of buses includes the state of use of each bus, and in a case where there is one bus for which a requested transfer destination and transfer size are allowed, said decision means decides that this bus should be used, and in a case where there are a plurality of buses for which a requested transfer destination and transfer size are allowed, said decision means decides to use preferentially a bus having the highest transfer speed.

14. A memory manager comprising:

a memory for supporting a burst mode in which a data transfer to successive locations is carried out; and

memory control means having a cache memory for

temporarily storing data exchanged with said memory;

wherein said memory control means prohibits data transfer to said memory using the cache memory if transfer of the data to said memory is performed in the burst mode, and permits data transfer to the memory through the cache memory if transfer of the data to said memory is performed in a single mode.

15. A memory manager comprising:

a memory for supporting a burst mode in which a data transfer to successive locations is carried out;

memory control means having a cache memory for temporarily storing data exchanged with said memory; and

a plurality of bus masters which access the memory;

wherein said memory control means transfers data to said memory directly without the intermediary of the cache memory, or transfers data to said memory upon first writing the data to the cache memory, in dependence upon the bus master that is to transfer the data to said memory.

16. The memory manager according to claim 15, wherein said memory control means has a rewritable table for storing identifiers of said bus masters in such a manner that it is possible to distinguish, for each identifier, whether data will be transferred to said memory directly without the intermediary of the cache memory or whether data will be transferred to said memory upon first being written to the cache memory;

data being transferred to said memory directly without the intermediary of the cache memory or data being transferred to said memory upon first being written to the cache memory, the transfer being made upon referring to the identifier of a bus master that is attempting to transfer data to said memory and to said table.

17. A power manager for controlling power consumption of an electric circuit which includes a plurality of circuit blocks controlled by a controller, comprising:

status monitoring means for monitoring operating status of each circuit block;

adding means for summing power consumed by each circuit block in the operating state; and

notification means for comparing summed power with a predetermined threshold value and, if the summed power exceeds the threshold value, so notifying the controller.

18. The power manager according 17, wherein said notification means has a plurality of mutually different values as threshold values and performs notification in dependence upon results of comparison with each of these threshold values.

19. The power manager according 17, further comprising timekeeping means for measuring elapsed time, wherein if a predetermined period of time elapses without any change in the operating state of each block after said notification means performs notification, said notification means

performs notification again.

20. The power manager according to claim 17, wherein the threshold value is rewritten by said controller.